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Sign Up

AMD Vivado Training

3 days (21 hours)

Overview

AMD Vivado is the industry-standard environment for designing, integrating, and validating modern FPGA designs, featuring synthesis, implementation, timing constraints, and hardware debugging. This training course guides you toward a more fluid and robust workflow with Vivado. Our AMD Vivado training course enables you to go beyond basic usage to master the key stages of an FPGA project, from design creation to bitstream generation. You will learn how to structure a project, effectively use the graphical user interface and Tcl, and manage IPs, XDC constraints, and timing analysis to ensure the reliability of your designs. Upon completion of the training, you will be able to improve your design cycles, better interpret synthesis and placement-routing results, and prepare a more stable design for production. This training also covers best practices in simulation, programming, debugging, and design methodology to enhance the quality of your projects on AMD platforms.

Like all our training courses, this one will introduce you to **the latest stable version** of the technology and its new features.

Objectives

- Understand the end-to-end AMD Vivado development workflow.
- Create and organize an FPGA project using a clear and reproducible method.
- Use the Vivado IDE and Tcl to automate common tasks.
- Define and verify XDC constraints to ensure timing compliance.
- Analyze the results of synthesis, placement, and bitstream generation.
- Implement validation and debugging practices tailored to a specific project context.

Target Audience

- FPGA Engineer
- Embedded Developer
- Electronics Designer

- System architect
- Digital Design Technician

Requirements

- Basic knowledge of digital logic and electronic design.
- Previous experience with a technical development environment or a CAD tool.
- Basic understanding of hardware description languages, such as VHDL or Verilog.
- General understanding of timing constraints and validation workflows.
- Ability to read technical documentation in English.

Technical Prerequisites

- A recent computer with sufficient RAM and disk space to install AMD Vivado.
- An operating system compatible with the selected version of the Vivado Design Suite.
- A stable network connection for installing components, licenses, and updates.
- A comfortable monitor for working with the IDE, reports, and debugging windows.
- For remote training, a microphone and headset to follow along with demonstrations and workshops.

AMD Vivado Training Program

[Day 1 - Morning]

Introduction to the Vivado

Workflow

- Overview of the AMD Vivado ecosystem and its applications in FPGA design.
- Overview of the RTL-to-bitstream flow, from source input to target programming.
- Getting started with the interface, project views, reports, and navigation areas.
- Differences between project mode and non-project mode, and their impact on workflow organization.
- Introduction to the concepts of synthesis, implementation, timing, and bitstream generation.
- Hands-on workshop: launching Vivado, creating your first project, and identifying the main work screens.

[Day 1 - Afternoon]

Project Creation and Structuring

- Adding HDL source files, constraint files, and hierarchy elements.
- Managing project settings, file sets, and synthesis options.
- Organizing IPs and understanding the reusable component catalog.

- Reading messages, alerts, and initial design quality indicators.
- Best practices for naming, organizing, and maintaining a shared project.
- Hands-on workshop: Import a simple design, configure the project, and verify source consistency.

[Day 2 - Morning]

Constraints and Timing

- Role of XDC files in the temporal and physical description of the design.
- Defining clocks, ports, and input and output delays.
- Reading timing reports and identifying critical paths.
- Understanding common constraints, such as false paths and multi-cycle paths.
- Impact of constraints on the quality of synthesis and implementation.
- Hands-on workshop: writing an initial set of XDC constraints and interpreting a timing report.

[Day 2 - Afternoon] Synthesis

and Implementation

- Overview of the synthesis process and interpretation of the results generated by the tool.
- Principles of placement and routing, including associated optimization criteria.
- Analysis of resource, congestion, and routing quality reports.
- Using schematic views and reports to identify areas of concern.
- Methodological approach for correcting a design and restarting an optimization cycle.
- Hands-on workshop: perform synthesis and implementation, then adjust the design based on the reports.

[Day 3 - Morning] Automation

and Integration

- Introduction to Tcl for automating repetitive tasks and ensuring the reliability of procedures.
- Using the Tcl Console and running scripts in the Vivado environment.
- Creating basic commands to generate, configure, and launch a workflow.
- Management of IPs, sources, and configuration variants using a scalable approach.
- Preparing a more robust workflow for teams and projects involving multiple repositories.
- Hands-on workshop: writing and running a simple Tcl script to launch a processing sequence.

[Day 3 - Afternoon]

Validation, programming, and debugging

- Generating the bitstream and preparing to program the target.
- Using Hardware Manager tools to detect and configure the board.
- Basic approaches to functional validation and post-implementation verification.
- Principles of hardware debugging and reading signals useful for diagnostics.
- Summary of best practices for securing an FPGA development workflow.
- Hands-on workshop: programming a test target and conducting a verification and diagnostic session.

Target Audience

This training is intended for both individuals and companies—large or small—seeking to train their teams in a new advanced IT technology or to acquire specific industry knowledge or modern methodologies.

Entry-Level Assessment

The pre-training assessment complies with Qualiopi quality standards. Upon final registration, the learner receives a self-assessment questionnaire that allows us to evaluate their estimated proficiency in various types of technologies, as well as their expectations and personal goals for the upcoming training, within the limits imposed by the selected format. This questionnaire also allows us to anticipate certain connection or internal security issues within the company (intra-company or virtual classroom) that could pose challenges for monitoring and ensuring the smooth running of the training session.

Teaching Methods

Hands-On Training: 60% Practical, 40% Theoretical. Training materials distributed in digital format to all participants.

Organization

The course alternates between theoretical input from the instructor—supported by examples and reflection sessions—and group work.

Assessment

At the end of the session, a multiple-choice quiz is administered to verify that participants have successfully acquired the skills.

Certification

A certificate will be issued to each trainee who has completed the entire training program.